HGST
a Western Digital company

# Storage Class Memories: Hardware and Programming Interfaces

Zvonimir Z. Bandic, Storage Architecture, HGST Research

https://www.usenix.org/conference/fast14/technical-sessions/presentation/vucinic

# Goals

- **What is driving the need for new programming models and hardware interfaces for SCM's?**
- **What are the most promising hardware interfaces and software protocols to talk to SCM's? How will they fit into the existing operating systems and programming language environments?**
- **What new protocols or primitives are needed in operating systems to support SCM's?**
- **What are the trajectories for various potential SCM technologies being derived from DRAM, FLASH, and other persistent SCM media types and how will they affect the required hardware and software interfaces and potential programming models?**
- **What kind of new applications are enabled by SCM's?**

# Driving need: PCM (and ReRAM, MRAM, etc)

### 1.4.1 PCM MATERIALS/DEVICE PHYSICS

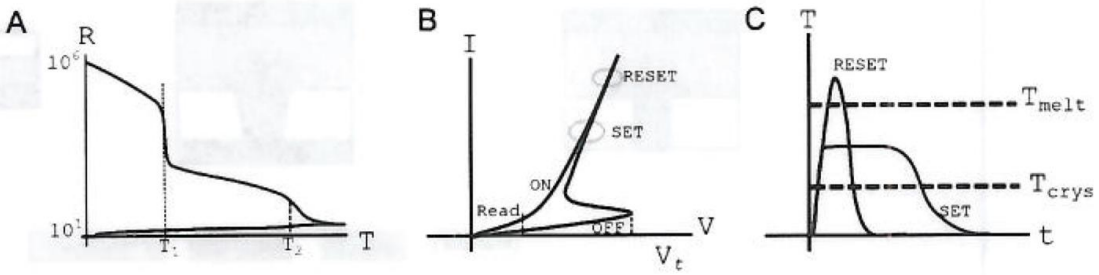
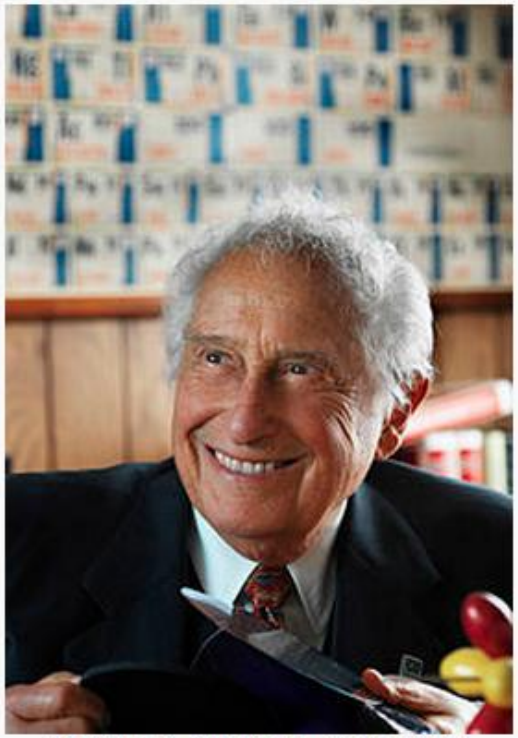



**Figure 1.9:** (A) Typical R-T (normalized) curve of chalcogenide films show that the resistivity of amorphous phase is 5 – 6 orders of magnitude higher than the polycrystalline phases. $T_1$ and $T_2$ are the temperatures where the transition to f.c.c and h.c.p phases take place. (B) I-V curves observed for PCM devices show that in the on state, the device behaves like a non-linear resistor. In the off state, the devices undergoes threshold switching at a critical bias ($V_t$). (C) Ideal thermal profiles generated within the cell during SET and RESET programming. (Adapted from [26, 209]). from Qureshi, Gurumurthi, Rajendran (2011)

- **Fast readout: 80 ns**
- **Slow writing: 10s to 100s of microseconds (1 kiB)**
- **Looks like DRAM on reads, like NAND flash on writes**
- **High endurance: > $10^7$ cycles**
- **Long retention: > 10 years**

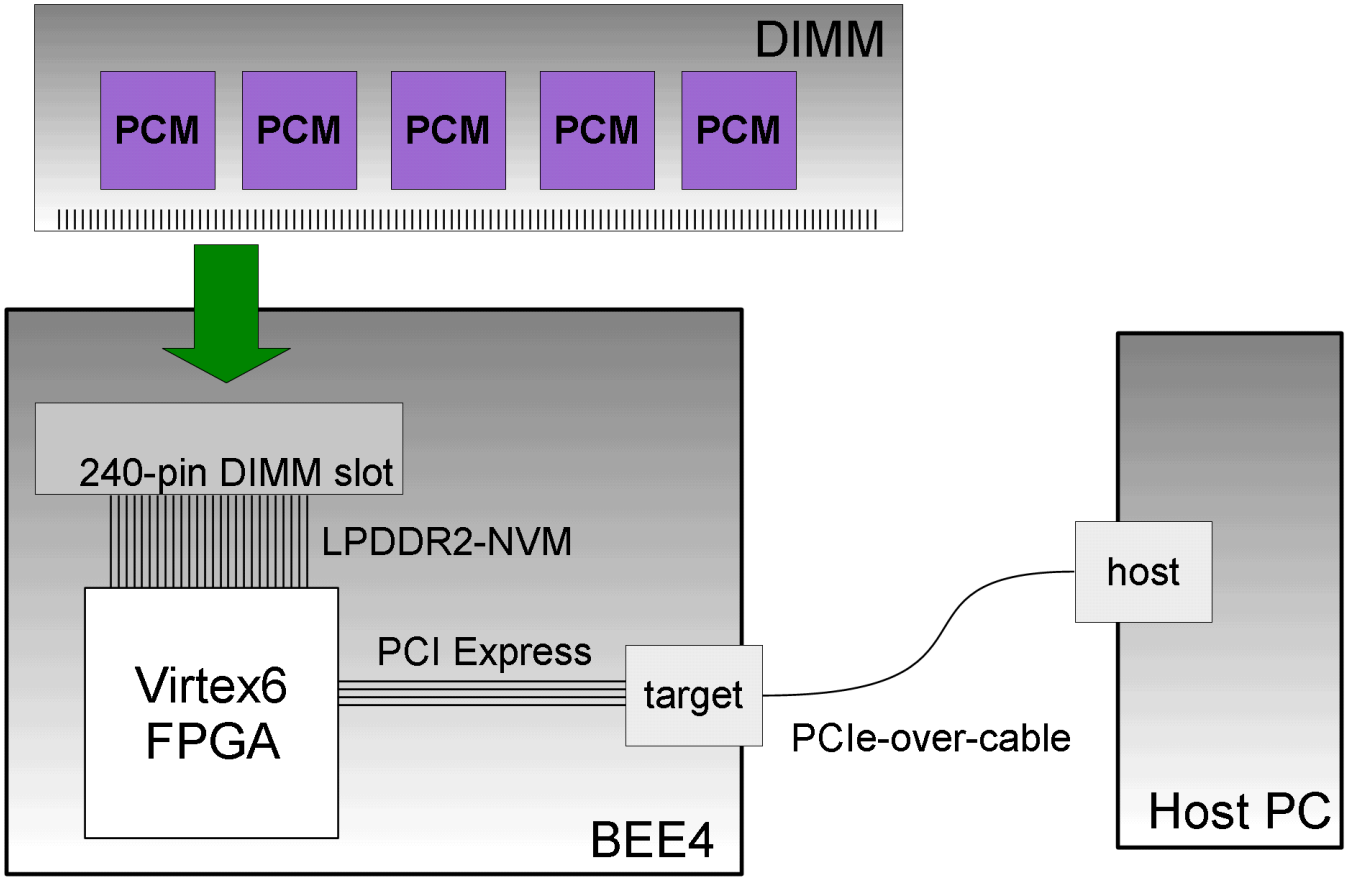
**Stanford Robert Ovshinsky**



Stanford R. Ovshinsky, August 2005

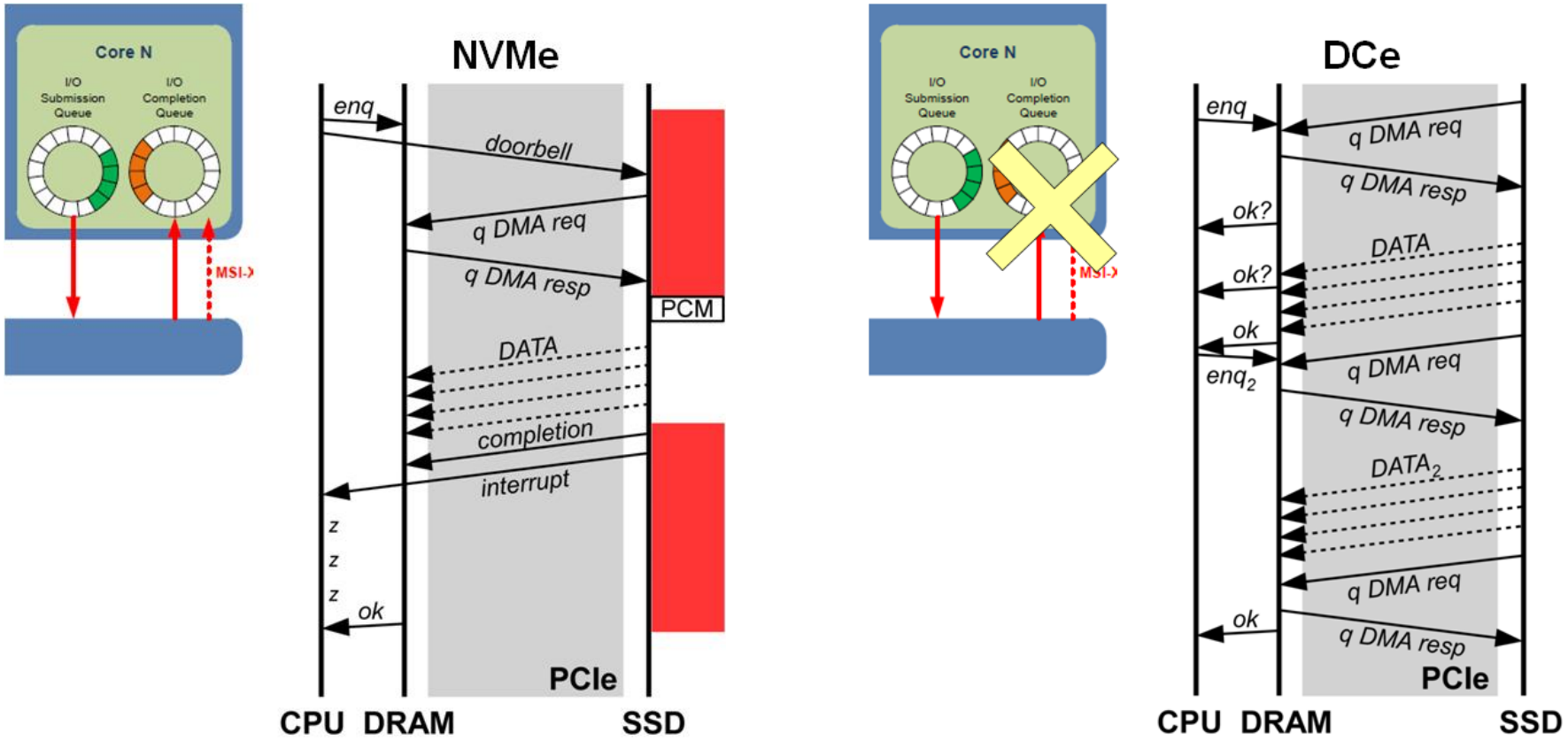
| | |
|---|---|
| **Born** | November 24, 1922<br>Akron, Ohio, U.S.A. |
| **Died** | October 17, 2012 (aged 89)<br>Bloomfield Hills, Michigan, U.S.A. |
| **Nationality** | American |
| **Occupation** | Inventor, scientist, and entrepreneur |
| **Known for** | Nickel–metal hydride battery |

# Hardware interfaces: DIMM vs. PCIe



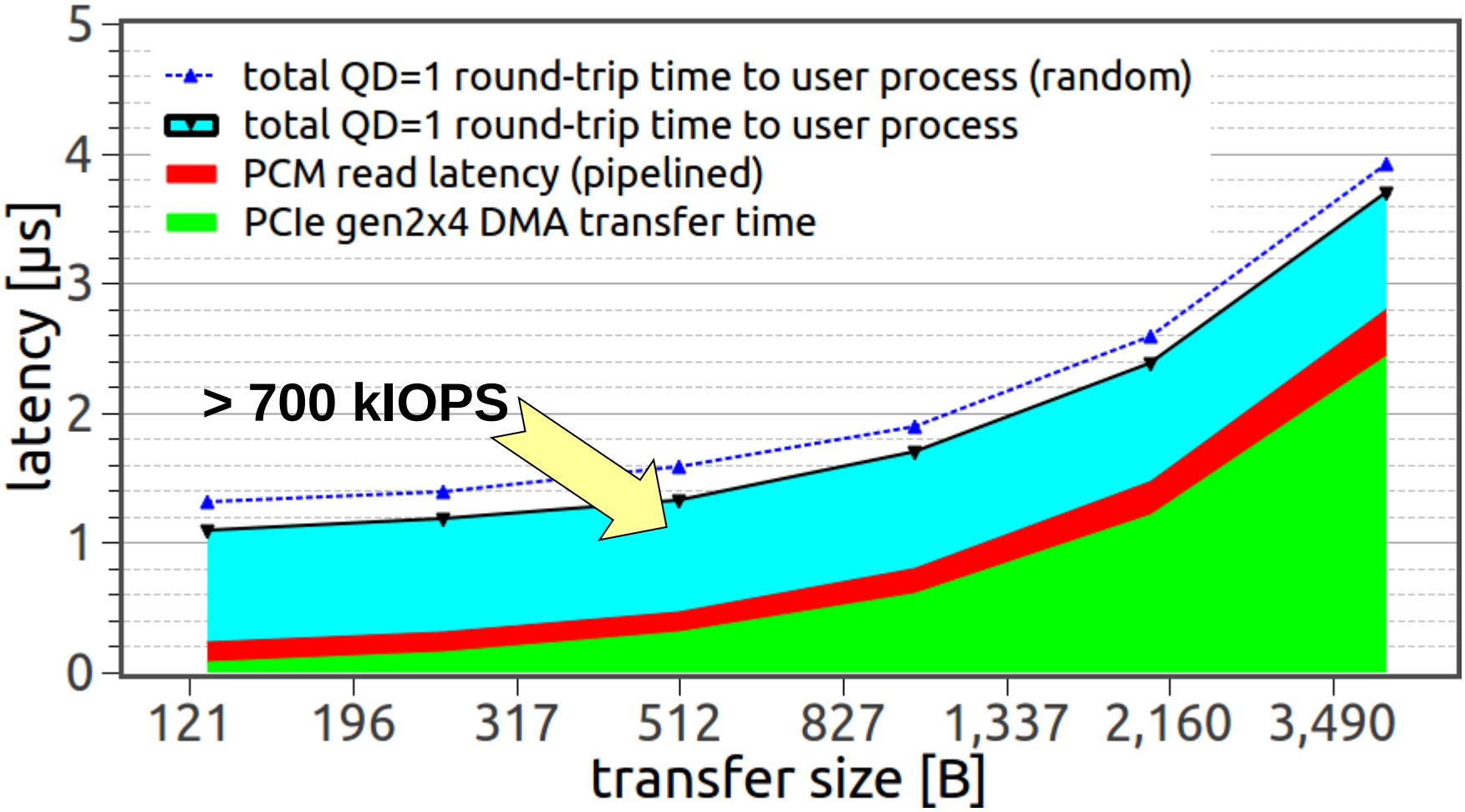

- **This also largely determinese how they will fit into the existing operating systems and programming language environments**

# New protocols: DCexpress




- **Poll from both ends of the slow link**
- **Infer completions by pre-filling receive buffer over the fast link**
- **https://www.usenix.org/conference/fast14/technical-sessions/presentation/vucinic**

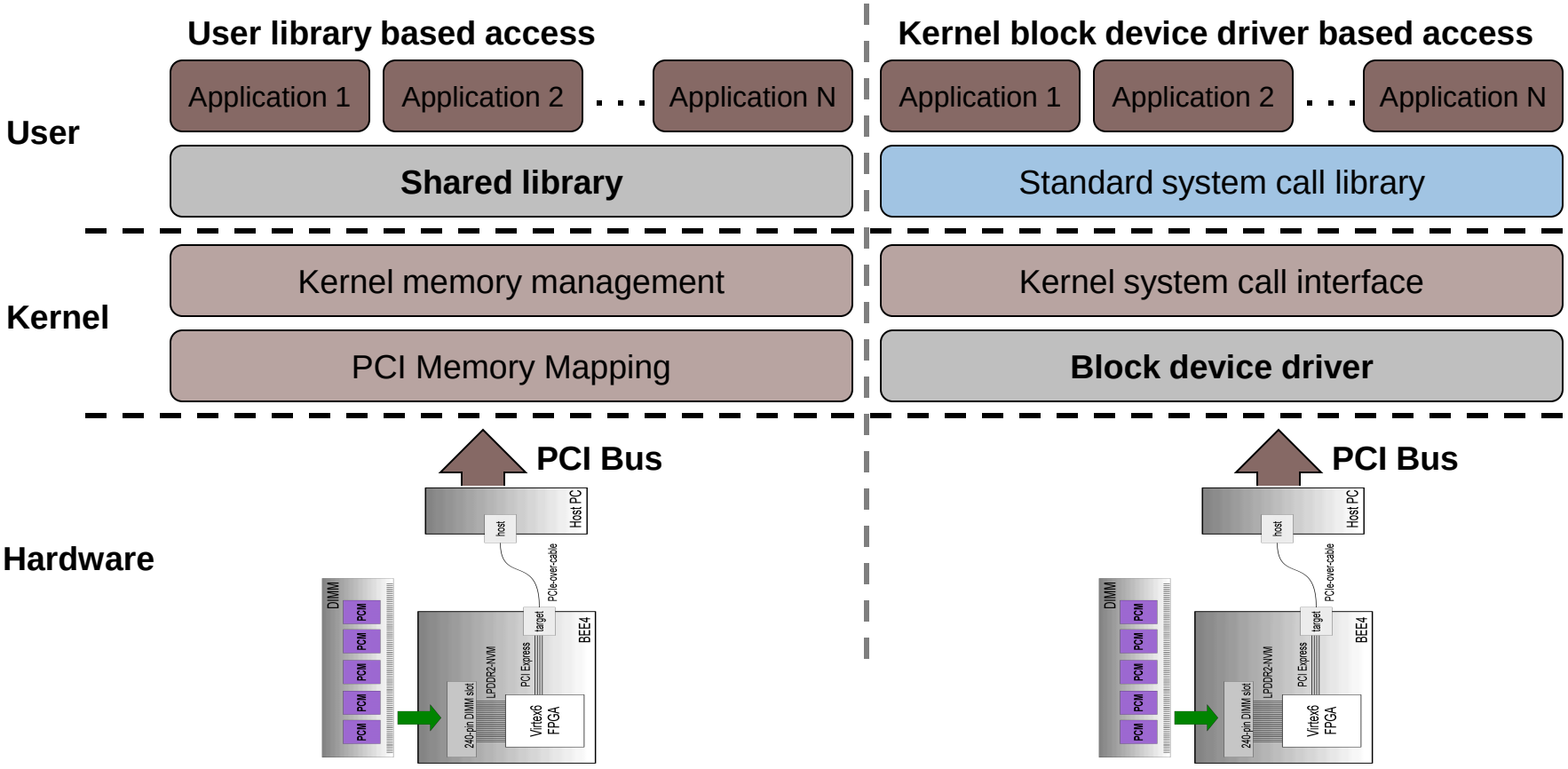
# DC Express




- Single user-space thread running on idle computer
- https://www.usenix.org/conference/fast14/technical-sessions/presentation/vucinic

# Interfaces/programming models

- **Two different paths**
  - User level library which provides non-standard API functions for read/write operations
  - Kernel level device driver which exposes the device as a block device accessible through standard system calls (read/write)



# New applications

- **Memory**
- **Storage class memory**
- **Improving SSDs:**
  - NV cache on SSD for endurance, performance, power...
- **NV caching on HDDs**
- **NV caching on HBAs**
- **L1, L2, L3 replacements/enhancement**

# Credits

- **https://www.usenix.org/conference/fast14/technical-sessions/presentation/vucinic**